Simulation # 10

**Flip-flop Circuits**



**Electronic circuits and devices simulation laboratory**

Department of Electrical engineering, NIT Rourkela

**Aim of the Expt**: Simulate and analyse different flip-flop circuits

**Objective:** Verify the Characteristics of different flip-flop circuits.

**Theory:**

In electronics, a flip-flopis a special type of gated latch circuit. There are several different types of flip-flops. The most common types of flip flops are:

**JK flip-flop**: A common variation of the SR flip-flop. A JK flip-flop has two inputs, labeled *J* and *K.* The J input corresponds to the SET input in an SR flip-flop, and the K input corresponds to the RESET input.

The difference between a JK flip-flop and an SR flip-flop is that in a JK flip-flop, both inputs can be HIGH. When both the J and K inputs are HIGH, the Q output is *toggled*, which means that the output alternates between HIGH and LOW.

For example, if the Q output is HIGH when the clock is triggered and J and K are both HIGH, the Q output is set to LOW. If the clock is triggered again while J and K both remain HIGH, the Q output is set to HIGH again, and so forth, with the Q output alternating from HIGH to LOW at every clock tick.

**SR flip-flop:** Is similar to an SR latch. Besides the CLOCK input, an SR flip-flop has two inputs, labeled SET and RESET. If the SET input is HIGH when the clock is triggered, the Q output goes HIGH. If the RESET input is HIGH when the clock is triggered, the Q output goes LOW.

Note that in an SR flip-flop, the SET and RESET inputs shouldn’t both be HIGH when the clock is triggered. This is considered an invalid input condition, and the resulting output isn’t predictable if this condition occurs.

**D flip-flop:** Has just one input in addition to the CLOCK input. This input is called the DATA input. When the clock is triggered, the Q output is matched to the DATA input. Thus, if the DATA input is HIGH, the Q output goes HIGH, and if the DATA input is LOW, the Q output goes LOW.

Most D-type flip-flops also include S and R inputs that let you set or reset the flip-flop. Note that the S and R inputs in a D flip-flop ignore the CLOCK input. Thus, if you apply a HIGH to either S or R, the flip-flop will be set or reset immediately, without waiting for a clock pulse.

**T flip-flop:** Thisis simply a JK flip-flop whose output alternates between HIGH and LOW with each clock pulse. Toggles are widely used in logic circuits because they can be combined to form counting circuits that count the number of clock pulses received.

T flip-flop can be obtained from a D flip-flop by connecting the Q-bar output directly to the D input. Thus, whenever a clock pulse is received, the current state of the Q output is inverted (that’s what the Q-bar output is) and fed back into the D input. This causes the output to alternate between HIGH and LOW. Similarly, a T flip-flop can be synthesised from a JK flip-flop simply by hard-wiring both the J and K inputs to HIGH. When both J and K are HIGH, the JK flip-flop acts as a toggle.

**Simulation of JK flip-flop:**

**Procedure:**

**1 (a)** Draw the given circuit using JK\_FF and Function generator.

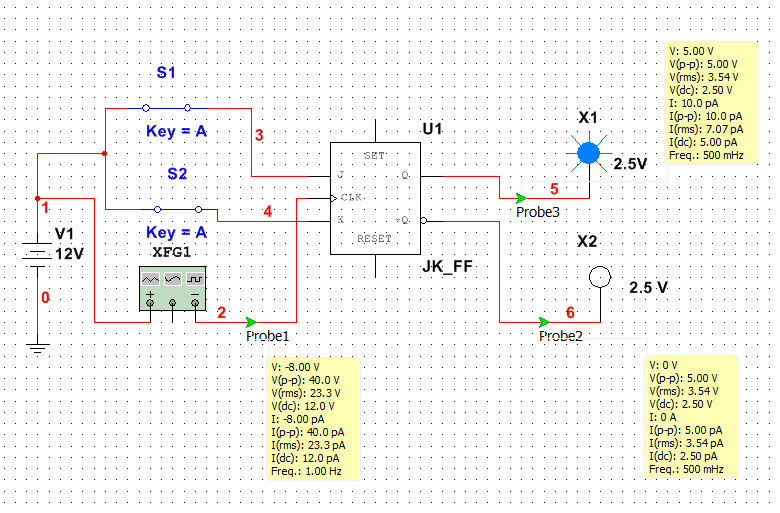
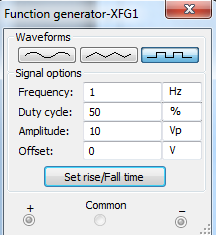
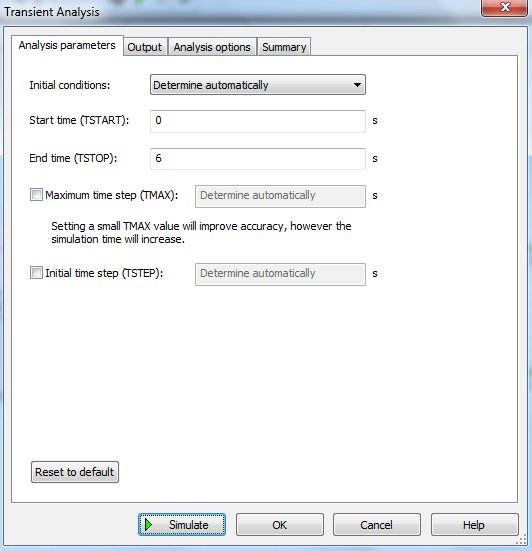
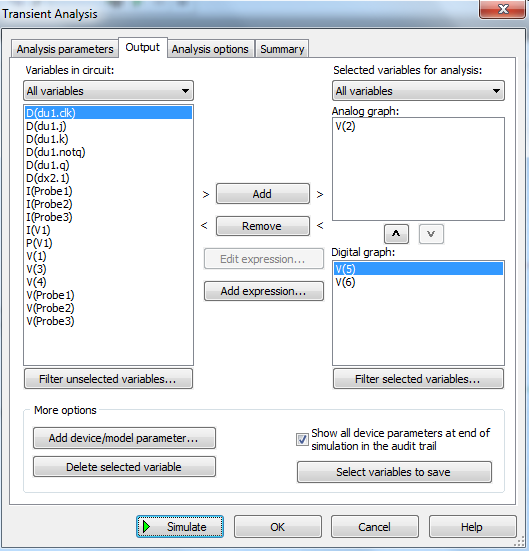


Fig. -1 (JK flip-flop circuit)

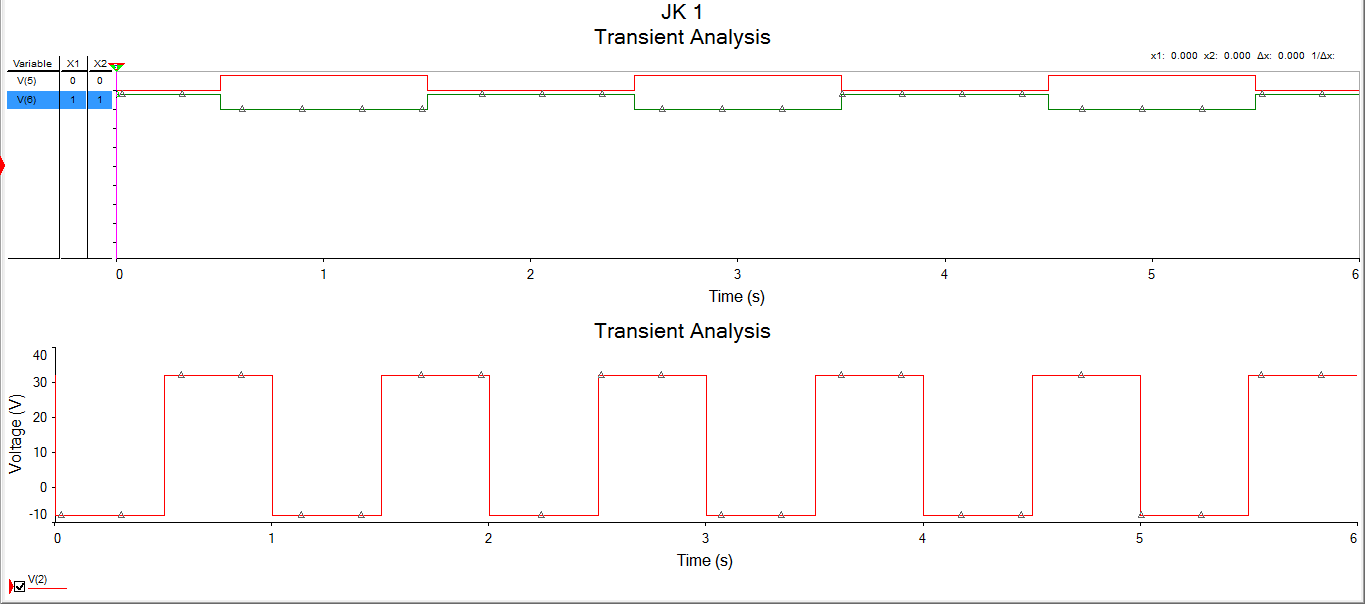
**(b)** Function generator settings:

**(c)** Input signal and Output parameters setting:



**(d).** Input and Output waveforms:



**2(a)** Draw the Digital counter circuit using JK\_FF as shown in fig -2.

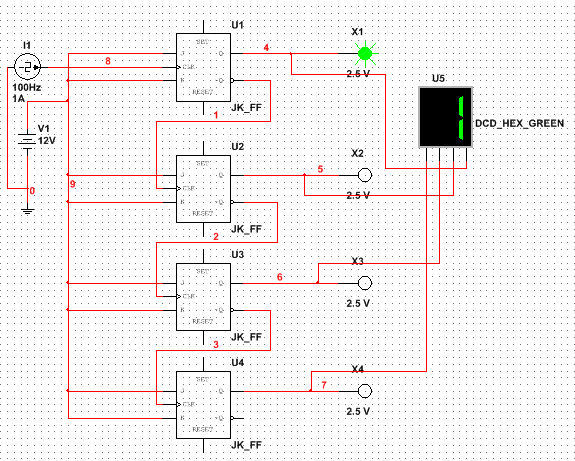
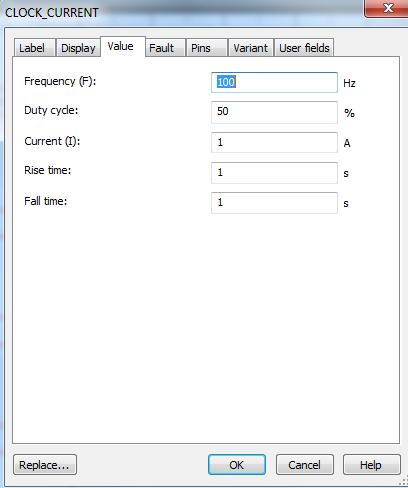


Fig. -2 (Digital counter circuit using JK\_FF)

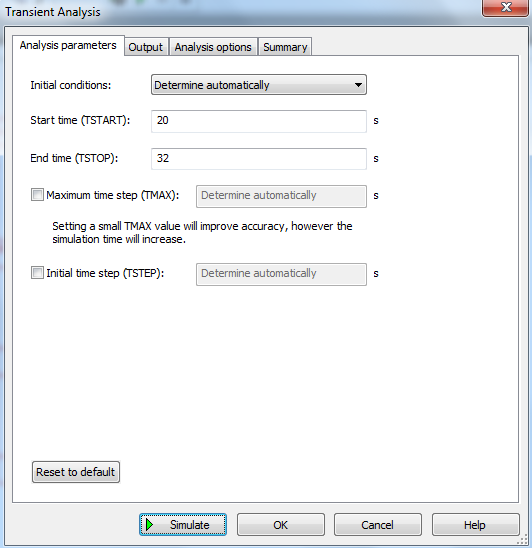
**(b). Clock current setting:** Set the values of clock current source as given in fig. 3



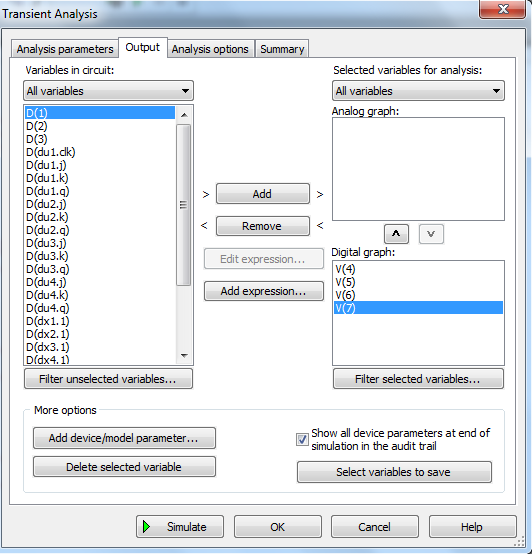
(Fig. -3, Clock current setting)

**(c)** Simulate the circuit and wait for a time of 20 seconds then observe the reading of 7-segment display.

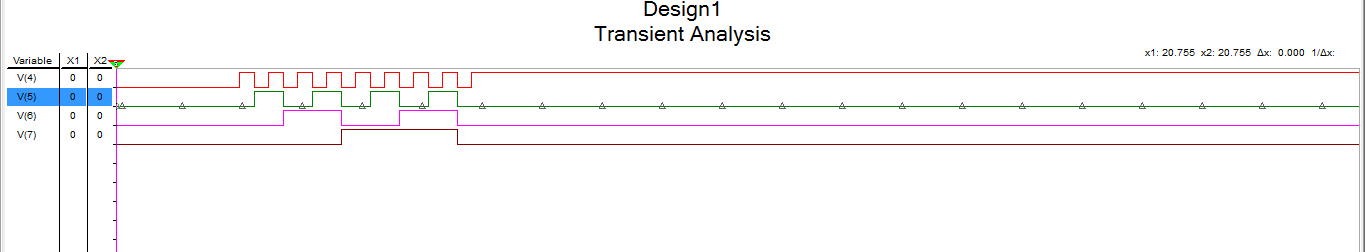
**(d)** Parameters setting:



**(e)** Output parameters setting:



**(f)** Output waveforms for counting 1:



**(g)** Simulate similar circuit using 4 channel Oscilloscope (XSC1) as shown in fig – 4, Fig-5, and fig-6

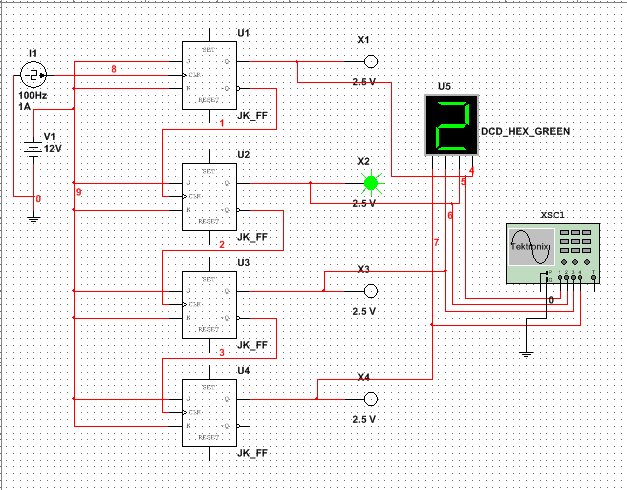


Fig. -4 (Digital counter circuit of JK\_FF using 4 channel Oscilloscope)

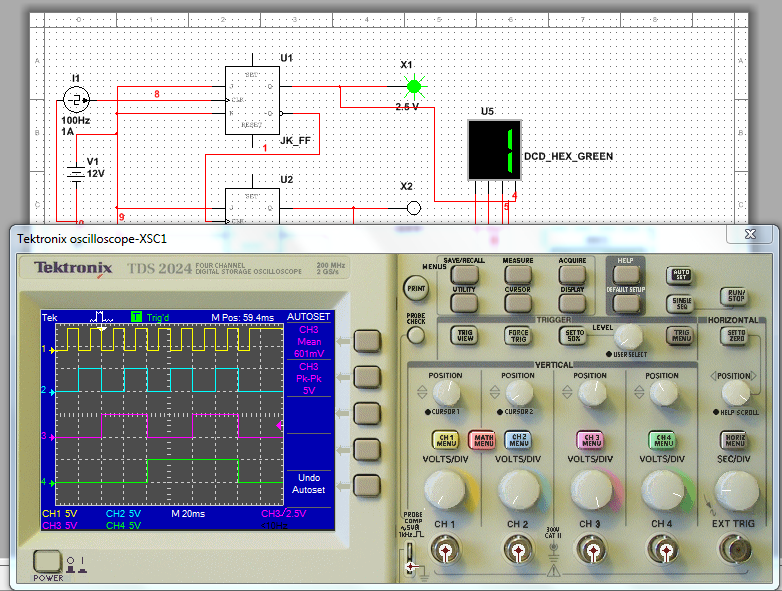


Fig. -5 (Output wave forms of Digital counter circuit for counting -1)

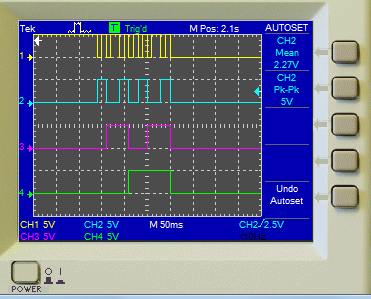
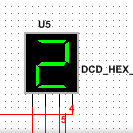
 

Fig. -6 (Output wave forms of Digital counter circuit for counting -2)

**Questions:**

1. Simulate SR flip-flop, D flip-flop and T flip-flop circuit as per the above given procedure and compare their Input and Output wave forms with truth table.
2. Connect the Set and Reset pin of JK\_FF circuit given in fig -1 with S1 and S2 separately and simultaneously. Compare the Input and Output wave forms.
3. Simulate the Input and Output wave forms of Digital counter circuit for counting the no. 3 to 9 and letter A, B, and C with graphical method and using Oscilloscope.

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